



Description

The FIR40N10BPG uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

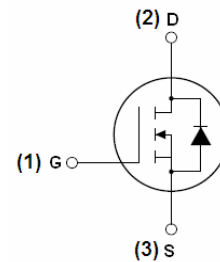
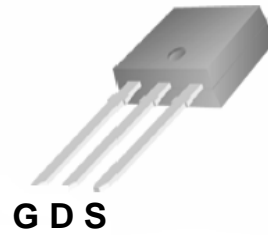
General Features

- $V_{DS} = 100V, I_D = 40A$
 $R_{DS(ON)} < 17m\Omega @ V_{GS}=10V$ (Typ:14m Ω)
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

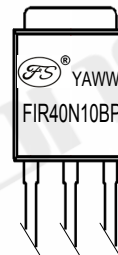
Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

PIN Connection TO-251



Marking Diagram



- Y = Year
- A = Assembly Location
- WW = Work Week
- FIR40N10BP = Specific Device Code

Package Marking And Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FIR40N10BP	FIR40N10BPG	TO-251	-	-	-

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	40	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	28	A
Pulsed Drain Current	I_{DM}	160	A
Maximum Power Dissipation	P_D	140	W
Derating factor	-	0.94	W/°C
Single pulse avalanche energy (Note 5)	E_{AS}	520	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C



Thermal Characteristic

Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	1.07	$^{\circ}C/W$
--	-----------------	------	---------------

Electrical Characteristics (TA=25°C unless otherwise noted)

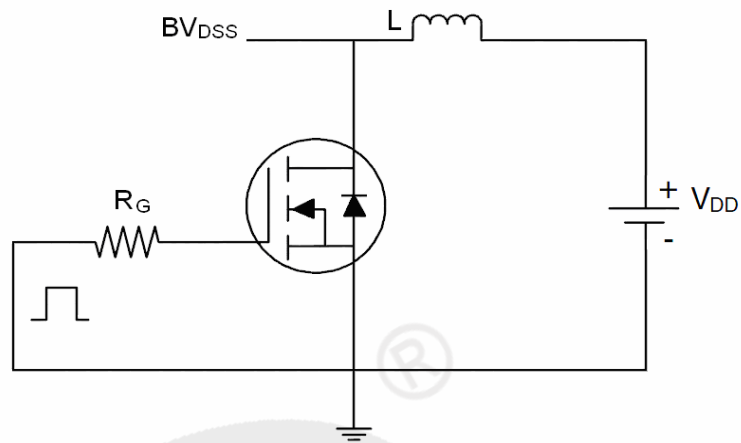
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=28A$	-	14	17	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=25V, I_D=28A$	32	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	3400	-	PF
Output Capacitance	C_{oss}		-	290	-	PF
Reverse Transfer Capacitance	C_{rss}		-	221	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=15\Omega,$ $R_G=2.5\Omega, V_{GS}=10V$	-	15	-	nS
Turn-on Rise Time	t_r		-	11	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	52	-	nS
Turn-Off Fall Time	t_f		-	13	-	nS
Total Gate Charge	Q_g		-	94	-	nC
Gate-Source Charge	Q_{gs}	$I_D=30A, V_{DD}=30V, V_{GS}=10V$	-	16	-	nC
Gate-Drain Charge	Q_{gd}		-	24	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=28A$	-	0.85	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	40	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 28A$	-	33		nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$ (Note3)	-	54		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

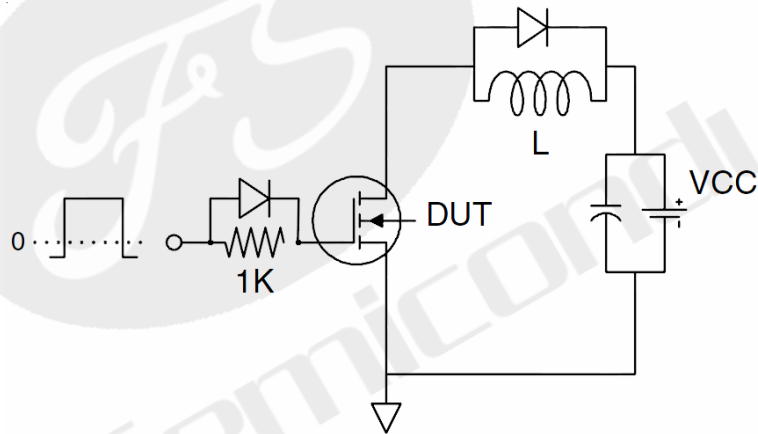
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuit

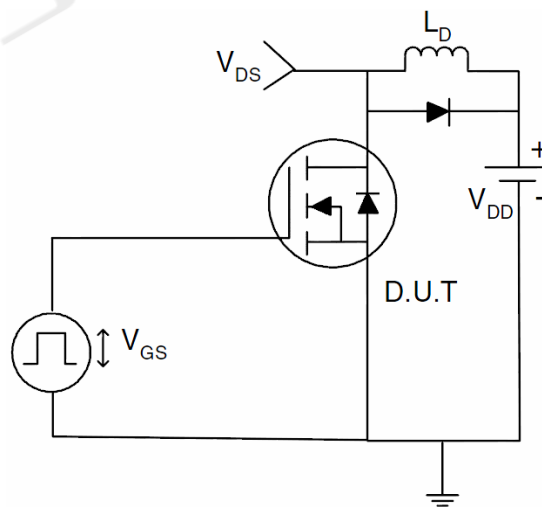
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:





Typical Electrical And Thermal Characteristics(Curves)

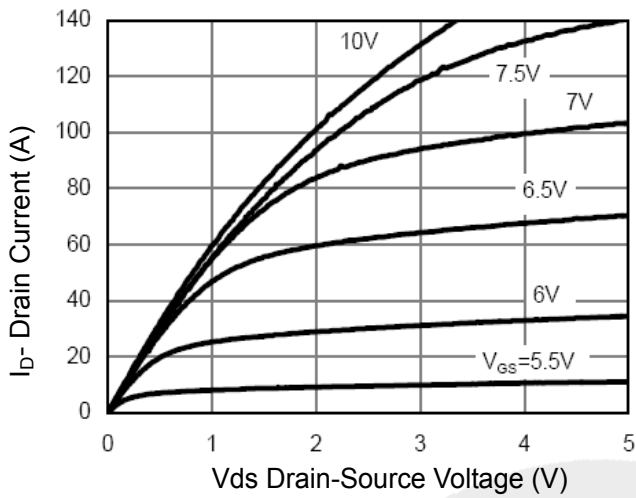


Figure 1 Output Characteristics

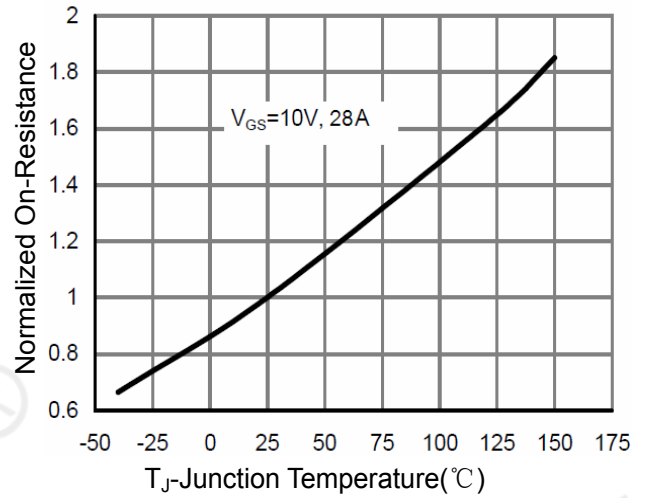


Figure 4 Rdson-Junction Temperature

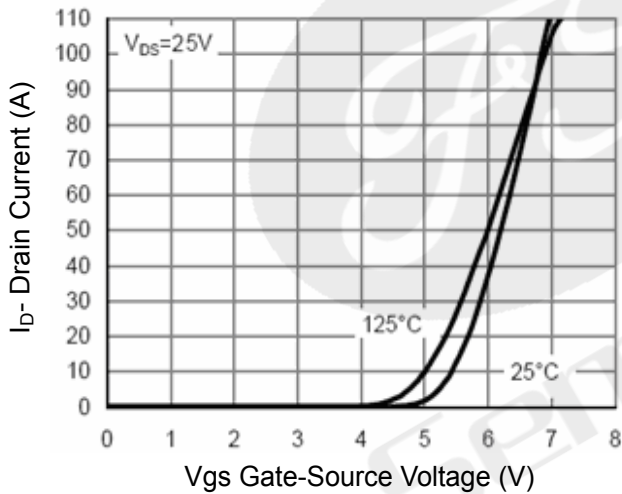


Figure 2 Transfer Characteristics

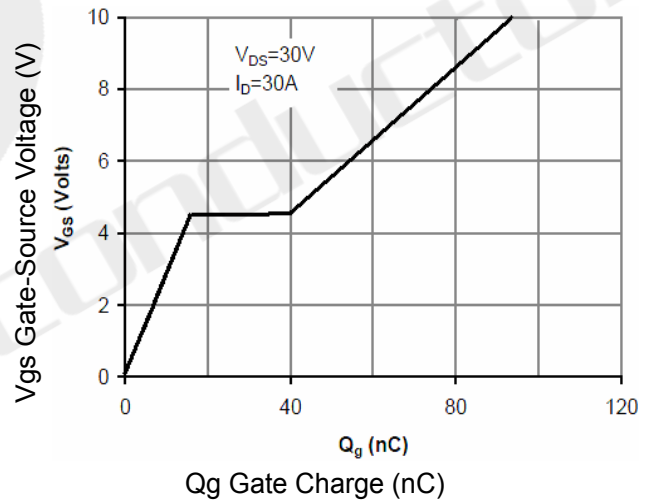


Figure 5 Gate Charge

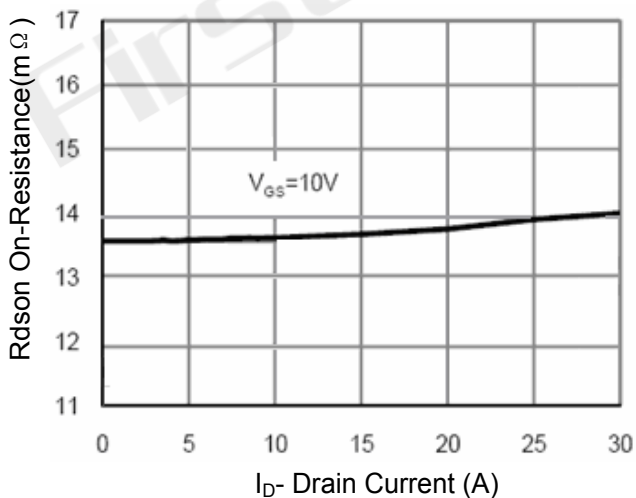


Figure 3 Rdson- Drain Current

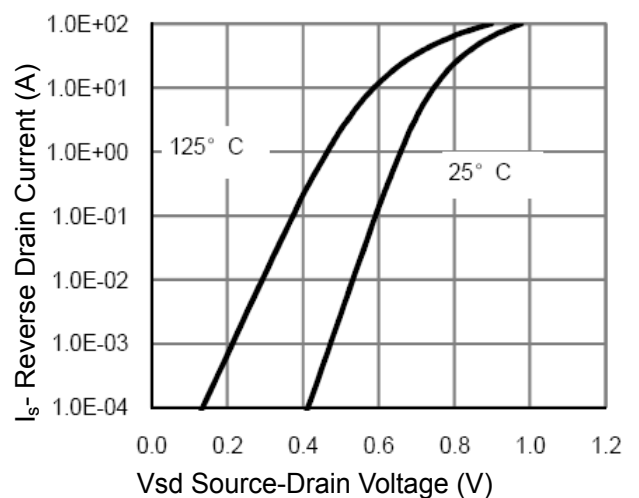


Figure 6 Source- Drain Diode Forward

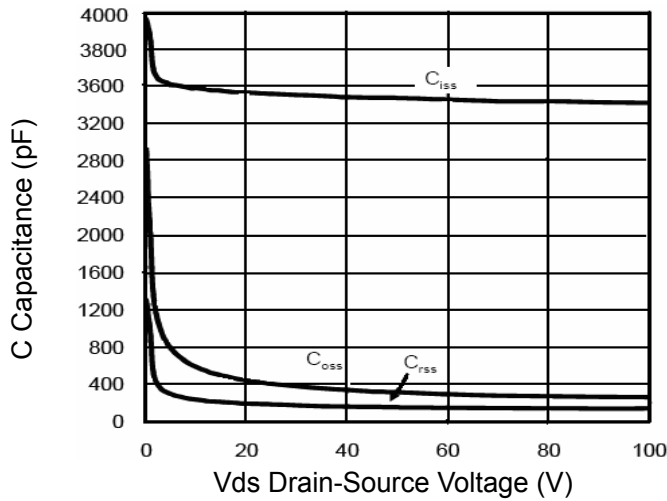


Figure 7 Capacitance vs Vds

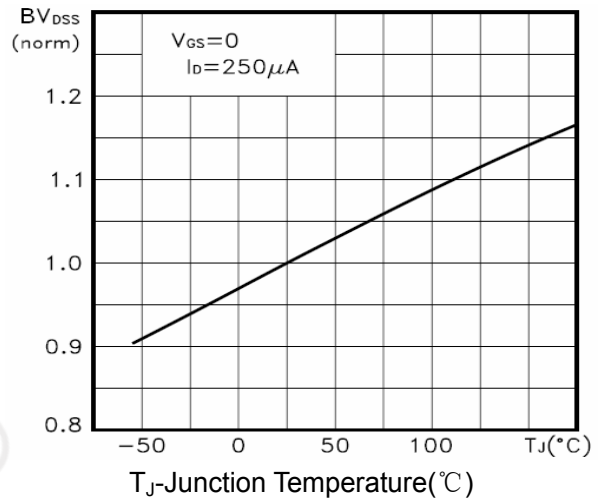


Figure 9 BV_{DSS} vs Junction Temperature

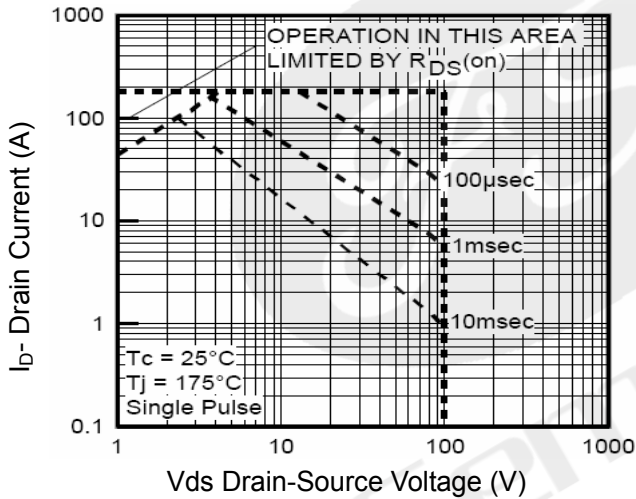


Figure 8 Safe Operation Area

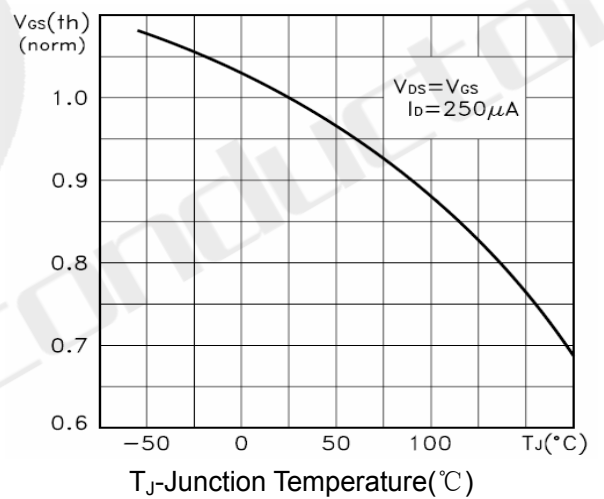


Figure 10 $V_{GS(th)}$ vs Junction Temperature

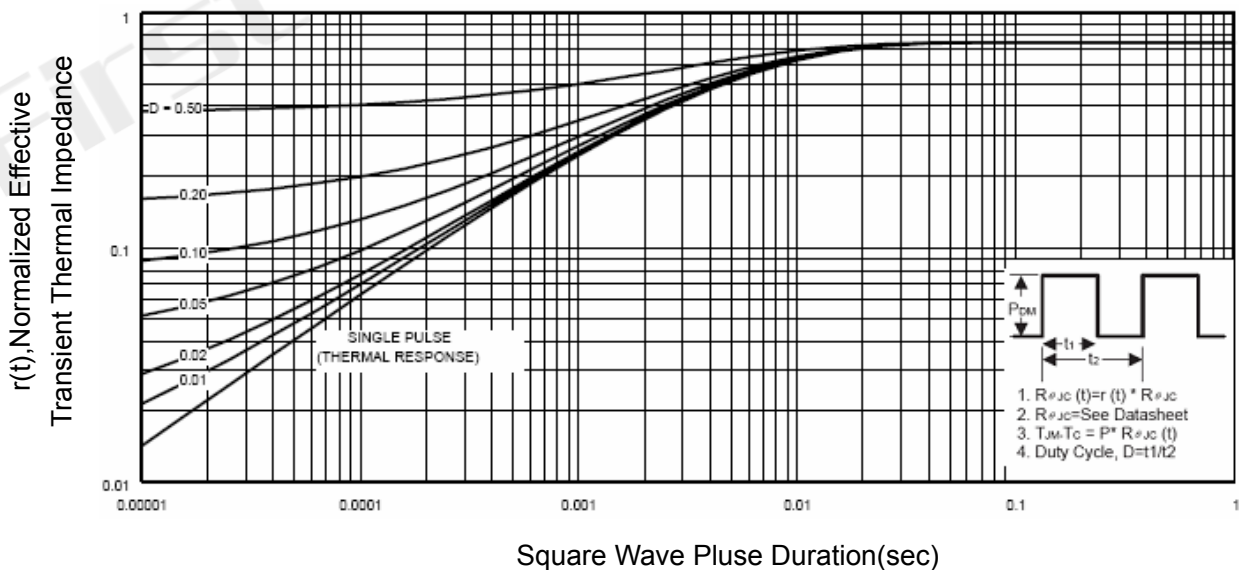
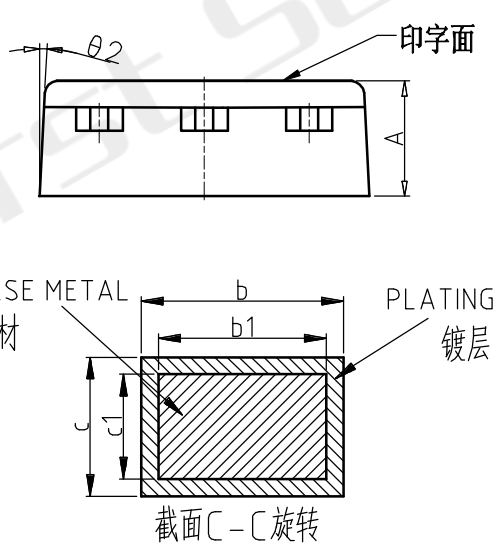
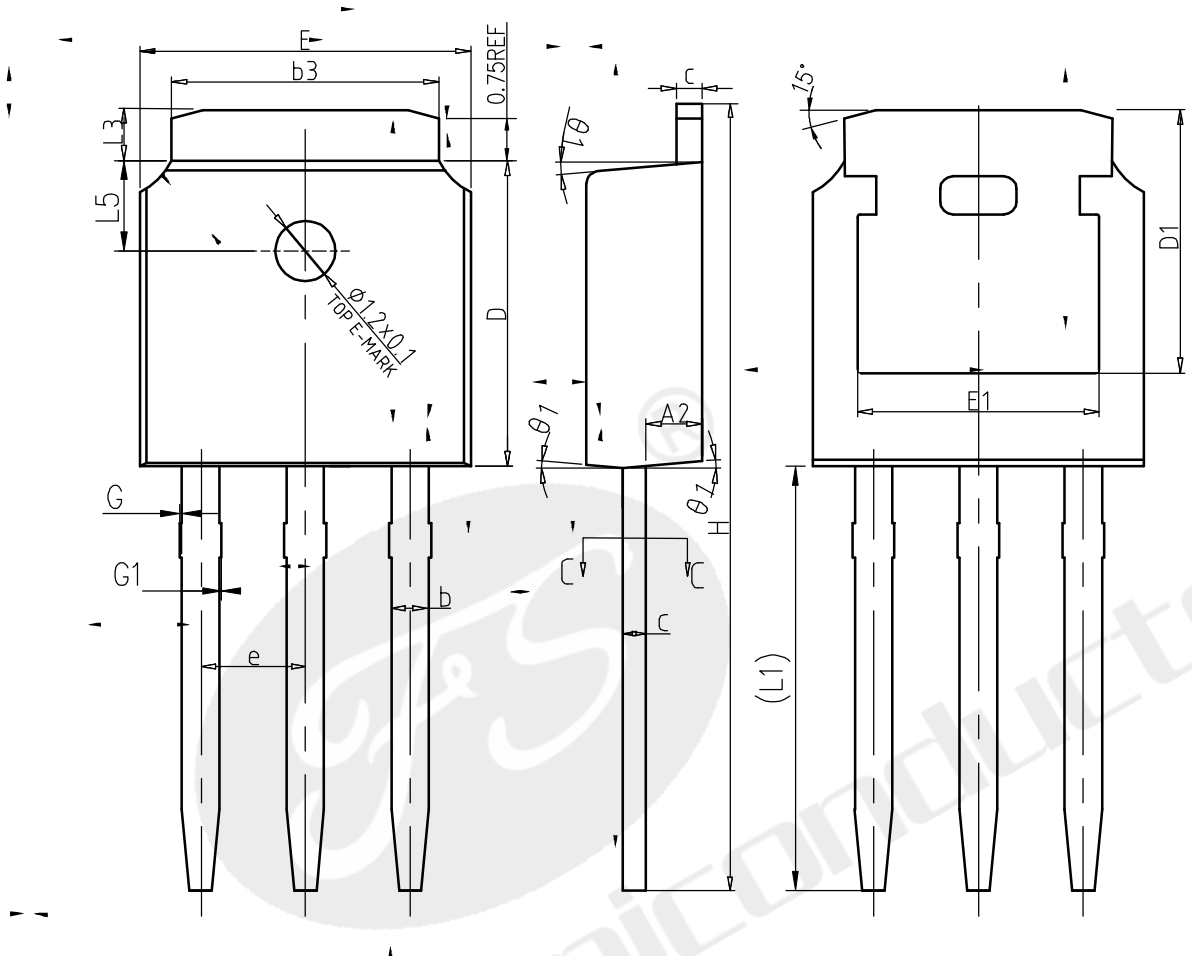


Figure 11 Normalized Maximum Transient Thermal Impedance



Package Information



COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	16.10	16.40	16.60
L1	9.20	9.40	9.60
L3	0.90	1.02	1.25
L5	1.70	1.80	1.90
θ 1	5°	7°	9°
θ 2	5°	7°	9°

NOTES

1.ALL DIMENSIONS REFER TO JEDEC STANDARD TO-251 AA, DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.



Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure, The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing, To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	