AP100N20MP

200V N-Channel Enhancement Mode MOSFET

Description

The AP100N20MP uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

V_{DS} = 200V I_D =100A

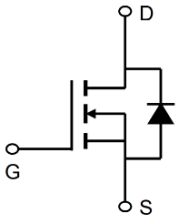
$R_{DS(ON)}$ < 20mΩ @ V_{GS}=10V **(Type：17mΩ)**

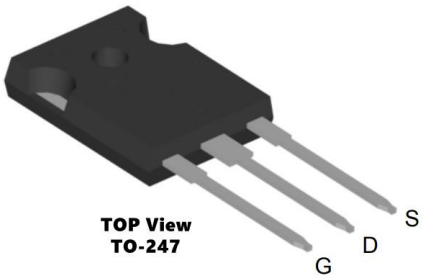
Application

Load Switch

PWM Application

Power management





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP100N20MP	TO-247-3L	AP100N20MP XXX YYYY	360

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDSS	Drain-to-Source Voltage	200	V
ID@TA=25℃	Continuous Drain Current VGS @ 10V	100	A
ID@TA=70℃	Continuous Drain Current VGS @ 10V	52	A
IDM[a1]	Pulsed Drain Current (pulse width limited by T_{JM})	300	A
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Energy	300	mJ
EAra1	Avalanche Energy, Repetitive	75	mJ
IAR a1	Avalanche Current	45	A
dv/dt[a2]	Peak Diode Recovery dv/dt	5.0	V/ns
PD	Power Dissipation	375	W
TJ，Tstg	Operating Junction and Storage Temperature Range	150，–55 to 150	℃
RθJC	Thermal Resistance, Junction-to-Case	0.45	℃/ W
RθJA	Thermal Resistance, Junction-to-Ambient	60	℃/ W

200V N-Channel Enhancement Mode MOSFET

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VDSS	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	200	220	--	V
IDSS	Drain to Source Leakage Current	V_{DS}=200V, V_{GS}=0V,T_a=25℃	--	--	1.0	μA
		V_{DS}=200V, V_{GS}=0V,T_a=125℃	--	--	100	μA
IGSS(F)	Gate to Source Forward Leakage	V_{GS}=+20V	--	--	100	nA
IGSS(R)	Gate to Source Reverse Leakage	V_{GS}=-20V	--	--	-100	nA
RDS(ON)	Drain-to-Source On-Resistance	V_{GS}=10V, I_D=40A	--	17	20	mΩ
VGS(TH)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	3.6	4.5	5.0	V
gfs	Forward Trans conductance	V_{DS}=25V, I_D=40A	50	65	--	S
R_g	Gate Resistance	V_{GS}=0V V_{DS} open f=1.0MHz		1.3		Ω
Ciss	Input Capacitance	V_{GS}=0V V_{DS}=25V f=1.0MHz	--	7500	--	pF
Coss	Output Capacitance		--	500	--	pF
Crss	Reverse Transfer Capacitance		--	210	--	pF
td(ON)	Turn-on Delay Time	I_D=40A, V_{DS}=50V V_{GS}=10V, R_g=2.5Ω	--	45	--	ns
t_r	Rise Time		--	70	--	ns
td(OFF)	Turn-Off Delay Time		--	110	--	ns
tf	Fall Time		--	90	--	ns
Q_g	Total Gate Charge	I_D=40A, V_{DD}=100V V_{GS}=10V	--	85	--	nC
Qgs	Gate to Source Charge		--	15	--	nC
Qgd	Gate to Drain (“Miller”) Charge		--	25	--	nC
ISD	Continuous Source Current (Body Diode)		--	--	75	A
ISM	Maximum Pulsed Current (Body Diode)		--	--	300	A
VSD	Diode Forward Voltage	I_S=40A, V_{GS}=0V	--	--	1.2	V
trr	Reverse Recovery Time	I_S=30A,T_j=25℃，V_{DD}=50V dI$_F$/dt=100A/μs, V_{GS}=0V	--	110	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.55	--	uC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is TJ = 25°C, L=0.3mH, RG=25Ω, VDD=50V，VGS=10V

4、The ISD=40A,di/dt≤100A/us, VDD≤BVDS, Start TJ=25℃

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Characteristics Curve:

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

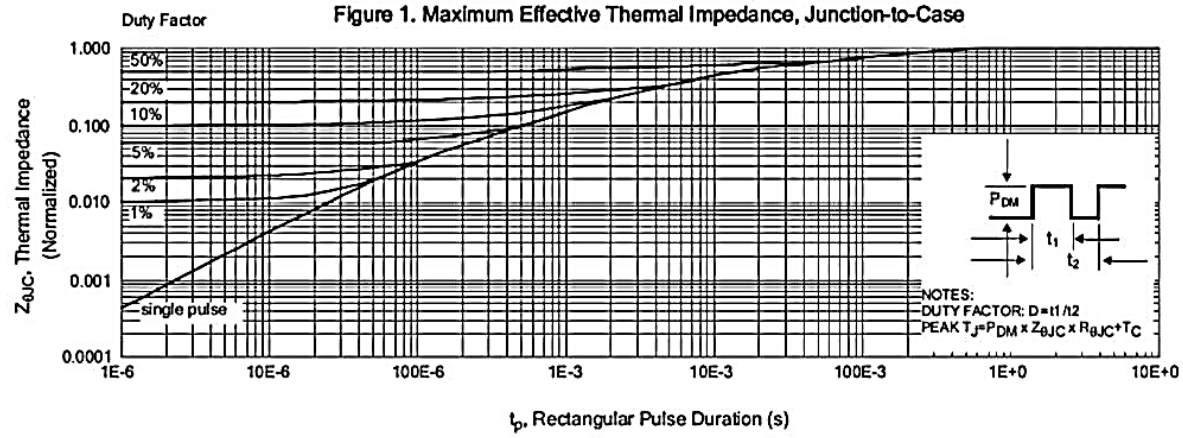


Figure 2 . Max. Power Dissipation vs Case Temperature

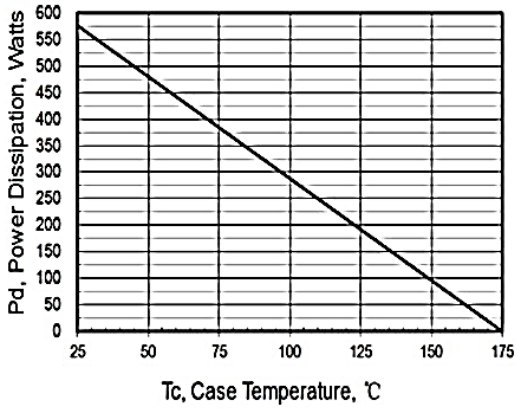


Figure 3 .Maximum Continuous Drain Current vs Tc

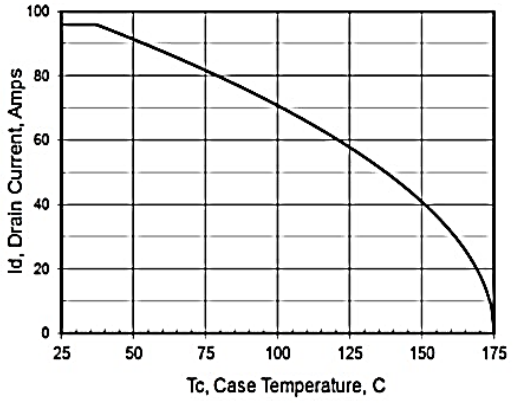


Figure 4. Typical Output Characteristics

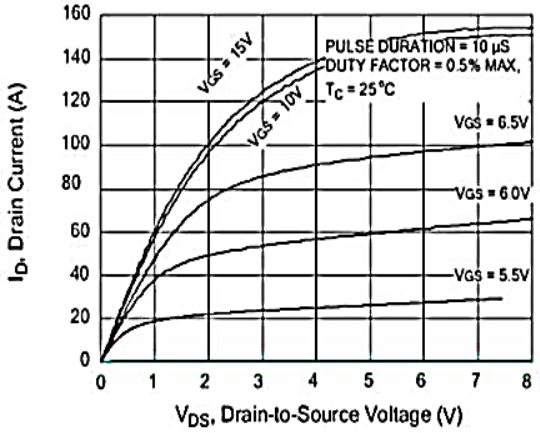


Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

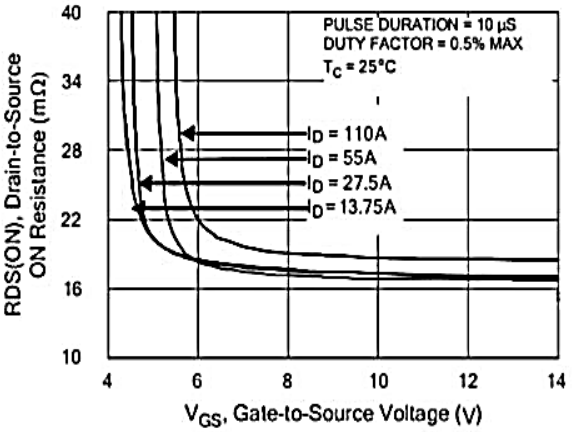


Figure 6. Peak Current Capability

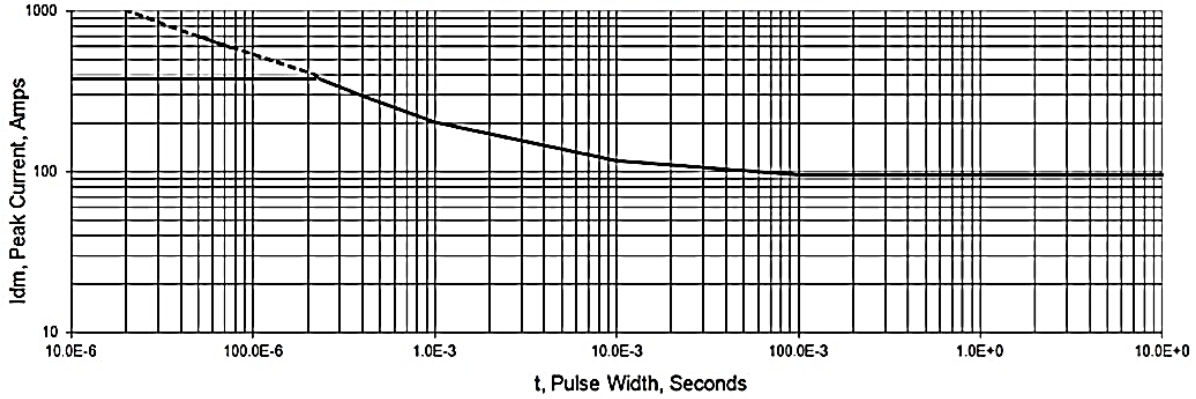


Figure 7. Typical Transfer Characteristics

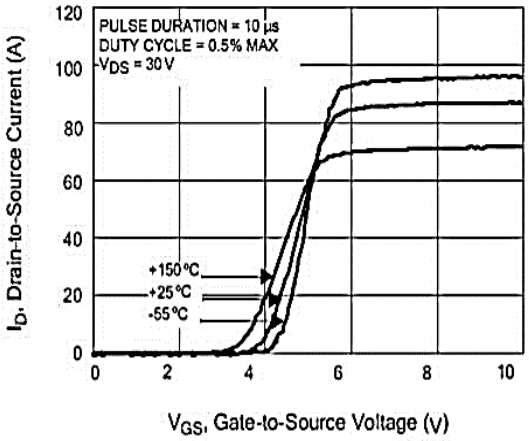


Figure 8. Unclamped Inductive Switching Capability

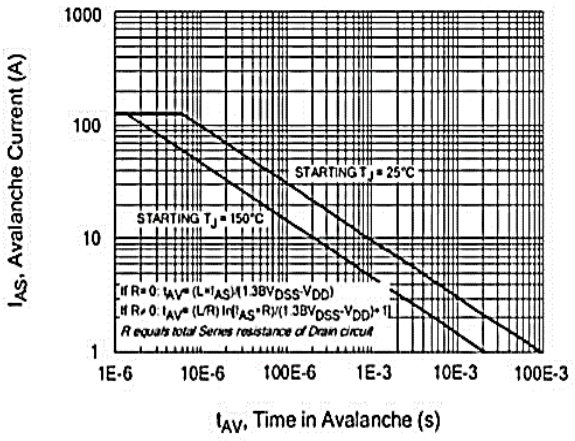


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

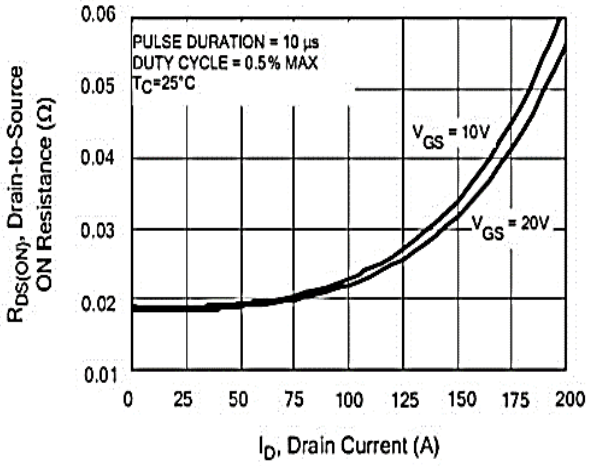


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

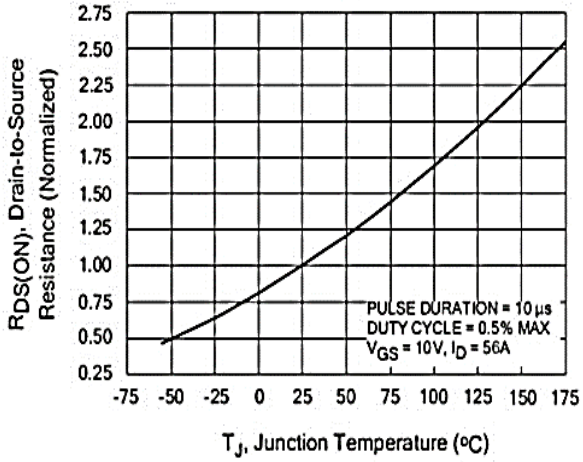


Figure 11. Typical Breakdown Voltage vs Junction Temperature

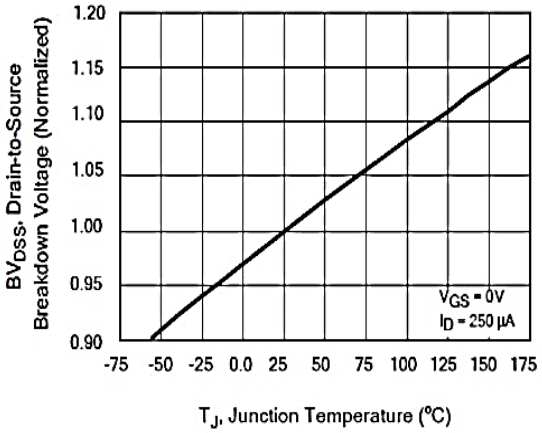


Figure 12. Typical Threshold Voltage vs Junction Temperature

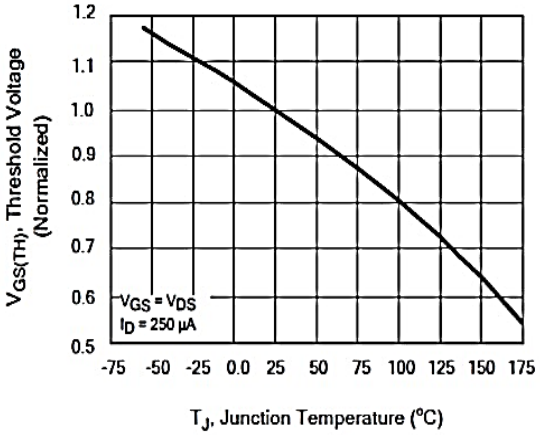


Figure 13 . Maximum Safe Operating Area

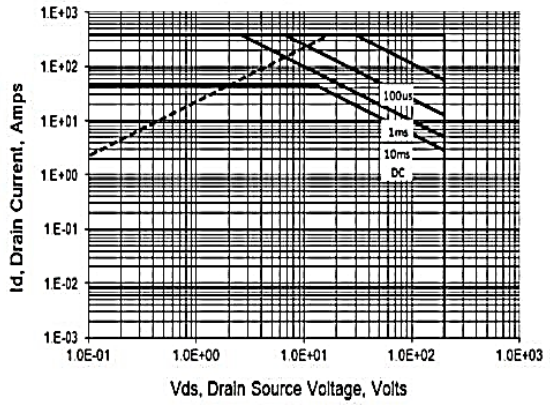


Figure 14. Capacitance vs Vds

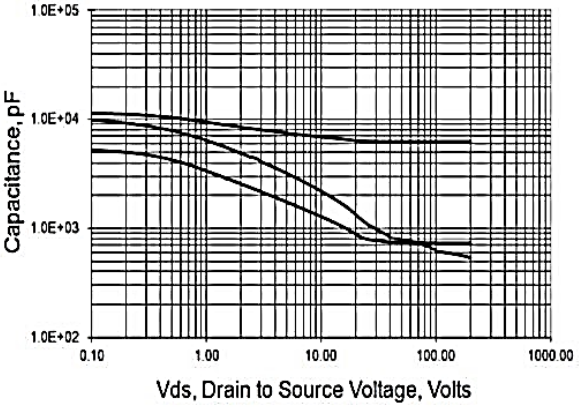


Figure 15 . Typical Gate Charge

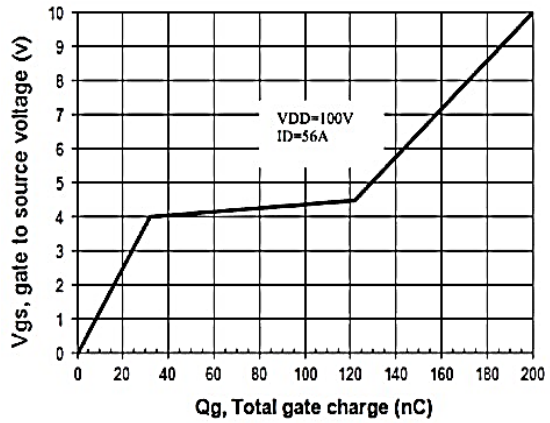
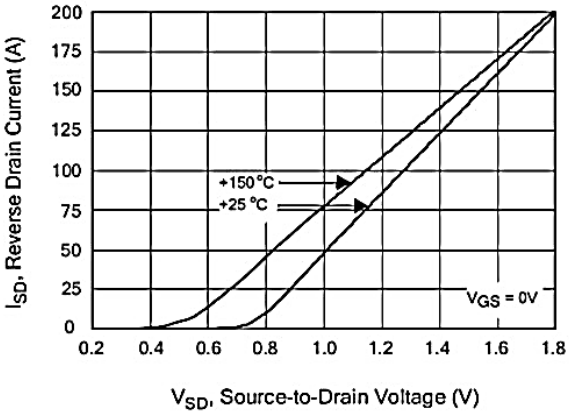
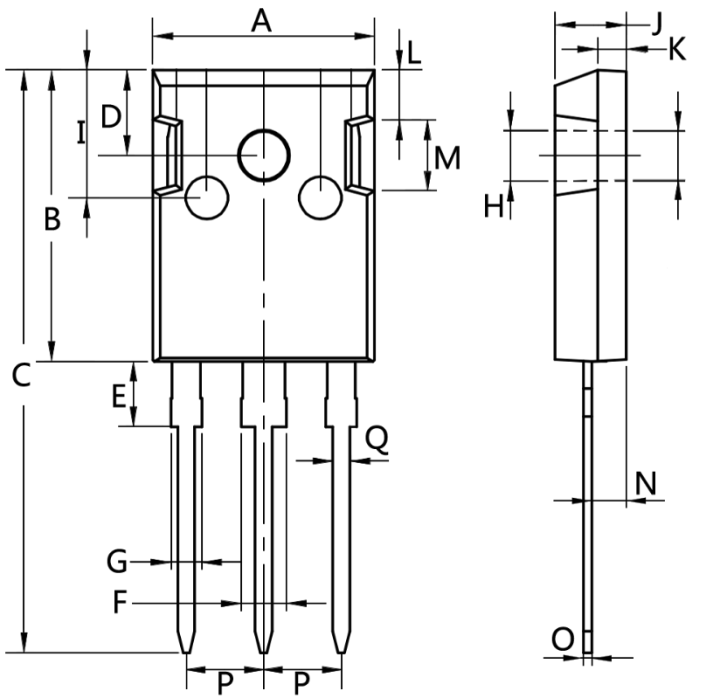


Figure 16. Typical Body Diode Transfer Characteristics



Package Mechanical Data-TO-247-3L



Dim.	Min.	Max.
A	15.0	16. 0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3